**SPIMaster Module Description Document**

**1. Introduction**  
The SPI Master module (hereinafter referred to as SPIM) has three signal lines: MISO, MOSI, and CLK. The SPIM module does not include an internal chip-select signal; during use, the SPI Slave can be selected by controlling a GPIO pin. A typical SPI interface connection for communication is shown in Figure 1.

The SPIM module has a dedicated internal DMA for data transfer, and it can generate an interrupt after the transmission is complete. The driver interface already implements both blocking and non-blocking transmit /receive interfaces.

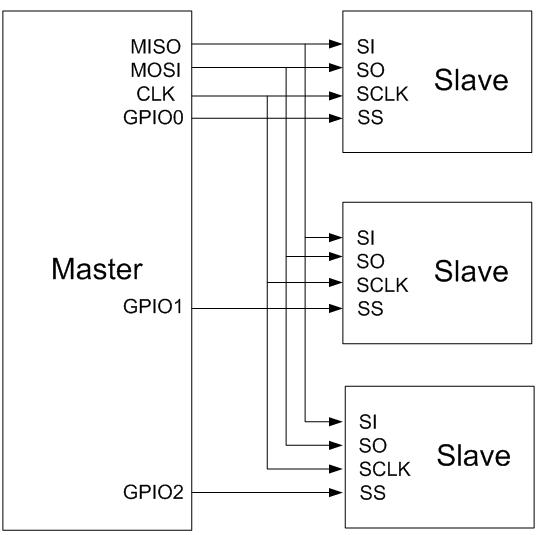


Figure 1 — SPI connection diagram

**2. Main Features**

Maximum supported clock speed: 24 MHz.

Supports four combinations of clock polarity and clock phase.

Internal dedicated DMA for data transfer.

Supports transmission-complete interrupts.